

REMARKS

The Office Action of September 10, 2009 was received and carefully reviewed.

Presently, claims 1-5 are amended to clarify the invention, and not for reasons of patentability. No claims have been hereby canceled, and no new claims have been added by way of this response. Accordingly, claims 1-15 are remain pending in the subject application..

Support for the amendment seen in independent claims 1-3 can be found at least in FIG. 10 of the application as originally filed. Thus, Applicants contend that neither the amendments to the claims nor the newly added claims include new matter.

Reconsideration and withdrawal of all currently pending rejections are hereby requested for least the reasons advanced in detail below.

Claim Rejections - 35 U.S.C. § 103

Claims 1-5 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hashimoto (U.S. Patent No.: 6,633,270 B2) (*Hashimoto*, hereinafter) in view of Yamazaki et al. (EP 1 058 310 A2) (*Yamazaki*, hereinafter). Applicants traverse this rejection for at least the reasons set forth below.

Independent claims 1-3, and the claims dependent therefrom, are patentably distinguishable over *Hashimoto* and *Yamazaki*, since *Hashimoto* and *Yamazaki*, taken either alone or in combination, fail to disclose, teach, or suggest each and every feature recited in the pending claims. For example, independent claim 1 (emphasis added) recites:

1. A display device comprising:
 - a plurality of source signal lines;
 - a plurality of gate signal lines;
 - a first power supply line in columns;**
 - a second power supply line in columns;**
 - a third power supply line in columns;**
 - a first power supply lines in rows;**
 - a second power supply lines in rows;**

a third power supply lines in rows; and

a plurality of pixels arranged in matrix, wherein the plurality of pixels includes a first pixel for red, a second pixel for green, and a third pixel for blue,

wherein each of the plurality of pixels includes a switching thin film transistor, a driving thin film transistor, and a light emitting element,

wherein the first pixel for red is connected to the first power supply line in columns, and the first power supply line in columns is connected to the first power supply line in rows,

wherein the second pixel for green is connected to the second power supply line in columns, and the second power supply line in columns is connected to the second power supply line in rows,

wherein the third pixel for blue is connected to the third power supply line in columns, and the third power supply line in columns is connected to the third power supply line in rows,

wherein the first power supply line in rows, the second power supply line in rows, and the third power supply line in rows are constructed to be supplied different voltages each other,

wherein an insulating thin film is formed in a portion under at least one of the plurality of source signal lines, the plurality of gate signal lines, the first power supply line in columns, the second power supply line in columns, the third power supply line in columns, the first power supply line in rows, the second power supply line in rows, and the third power supply line in rows.

Independent claim 2 (emphasis added) recites:

2. A method for manufacturing a display device comprising the steps of:

forming a plurality of source signal lines;

forming a plurality of gate signal lines;

forming a plurality of pixels arranged in matrix, wherein the plurality of pixels includes a first pixel for red, a second pixel for green, and a third pixel for blue, and wherein each of said plurality of pixels includes a switching thin film transistor, a driving thin film transistor, and a light emitting element;

forming a first power supply line in columns;

forming a second power supply line in columns;

forming a third power supply line in columns;

forming a first power supply line in rows;

forming a second power supply line in rows;

forming a third power supply lines in rows;

connecting the first pixel for red to the first power supply line in columns by a droplet discharging method or a printing method, wherein the first power supply line in columns is connected to the first power supply line in rows;

connecting the second pixel for green to the second power supply line in columns by a droplet discharging method or a printing method, wherein the second power supply line in columns is connected to the second power supply line in rows;
and

connecting the third pixel for blue to the third power supply line in columns by a droplet discharging method or a printing method, wherein the third power supply line in columns is connected to the third power supply line in rows,

wherein the first power supply line in rows, the second power supply line in rows, and the third power supply line in rows are constructed to be supplied different voltages each other.

Independent claim 3 (emphasis added) recites:

3. A method for manufacturing a display device comprising the steps of:

forming a source signal line;

forming a gate signal line;

forming a first power supply line in columns;

forming a second power supply line in columns;

forming a third power supply line in columns;

forming a first power supply line in rows;

forming a second power supply line in rows;

forming a third power supply line in rows;

forming a plurality of pixels arranged in matrix, wherein the plurality of pixels includes a first pixel for red, a second pixel for green, and a third pixel for blue, and wherein each of the plurality of pixels includes a switching thin film transistor, a driving thin film transistor, and a light emitting element; and

forming an insulating thin film in a portion under at least one of the source signal line, the gate signal line, the first power supply line in columns, the second power supply line in columns, the third power supply line in columns, the first power supply line in rows, the second power supply line in rows, and the third power supply line in rows,

wherein the first pixel for red is connected to the first power supply line in columns, and the first power supply line in columns is connected to the first power supply line in rows,

wherein the second pixel for green is connected to the second power supply line in columns, and the second power supply line in columns is connected to the second power supply line in rows,

wherein the third pixel for blue is connected to the third power supply line in columns, and the third power supply line in columns is connected to the third power supply line in rows, and

wherein the first power supply line in rows, the second power supply line in rows, and the third power supply line in rows are constructed to be supplied different voltages each other.

As seen above, independent claim 1 is directed to, *inter alia*, a display device including the features of a first power supply line in columns, a second power supply line in columns, a third power supply line in columns, a first power supply lines in rows, a second power supply lines in rows, a third power supply lines in rows, wherein the first pixel for red is connected to the first power supply line in columns, and the first power supply line in columns is connected to the first power supply line in rows, wherein the second pixel for green is connected to the second power supply line in columns, and the second power supply line in columns is connected to the second power supply line in rows, and wherein the third pixel for blue is connected to the third power supply line in columns, and the third power supply line in columns is connected to the third power supply line in rows. Applicants contend that neither *Hashimoto* nor *Yamazaki*, taken either alone or in combination, anticipate or render obvious at least the above-recited features with respect to present independent claim 1.

As also seen above, independent claim 2 is directed to, *inter alia*, the features of forming a first power supply line in columns, forming a second power supply line in columns, forming a third power supply line in columns, forming a first power supply line in rows, forming a second power supply line in rows, forming a third power supply lines in rows, connecting the first pixel for red to the first power supply line in columns by a droplet discharging method or a printing method, wherein the first power supply line in columns is connected to the first power supply line in rows, connecting the second pixel for green to the second power supply line in columns by a droplet discharging method or a printing method, wherein the second power supply line in columns is connected to the second power supply line in rows, and connecting the third pixel for blue to the third power supply line in columns by a droplet discharging method or a printing method, wherein the third power supply line in columns is connected to the third power supply line in rows. Applicants contend that neither *Hashimoto* nor *Yamazaki*, taken either alone or in combination, anticipate or render obvious at least the above-recited features with respect to present independent claim 2.

As further seen above, independent claim 3 is directed to, *inter alia*, the features of forming a first power supply line in columns, forming a second power supply line in columns, forming a third power supply line in columns, forming a first power supply line in rows, forming a second power supply line in rows, forming a third power supply line in rows, wherein the first pixel for red is connected to the first power supply line in columns, and the first power supply line in columns is connected to the first power supply line in rows, wherein the second pixel for green is connected to the second power supply line in columns, and the second power supply line in columns is connected to the second power supply line in rows, and wherein the third pixel for blue is connected to the third power supply line in columns, and the third power supply line in columns is connected to the third power supply line in rows. Applicants contend that neither *Hashimoto* nor *Yamazaki*, taken either alone or in combination, anticipate or render obvious at least the above-recited features with respect to present independent claim 3.

Hashimoto appears to disclose display device includes (a) a plurality of pixels arranged in a matrix, each of the pixels including a light-emitting device, a switch and a transistor, (b) a scanning line extending in a first direction, (c) a data line extending in a second direction perpendicular to the first direction, (d) a first bias voltage line extending in the second direction, (e) a bias voltage generating circuit which applies a bias voltage to the bias voltage line, (f) a second bias voltage line which surrounds the pixels and is a closed line, and (g) a third bias voltage line which electrically connects the bias voltage generating circuit to the second bias voltage line (see *Hashimoto*, e.g., the Abstract). However, *Hashimoto* fails to disclose, teach, or suggest the above-mentioned features recited in present independent claims 1-3.

Yamazaki appears to disclose that a part of or all of a gate electrode that overlaps with channel formation regions of a pixel TFT is caused to overlap with second wirings (source line or drain line), in order to increase an aperture ratio. Additionally, *Yamazaki* appears to disclose that a first interlayer insulating film and a second interlayer insulating film are disposed between the gate electrode and the second wirings so as to decrease a parasitic capacitance (see *Yamazaki*, e.g., the Abstract). Applicants assert that *Yamazaki* fails to make up for the above-recited deficiencies with respect to *Hashimoto*.

For at least the reasons stated above, neither *Hashimoto* nor *Yamazaki*, taken either alone or in combination, anticipate or render obvious each and every feature with respect to independent claims 1-3 as presently recited. Consequently, the Examiner has failed to provide a proper *prima facie* case of obviousness in the rejection of claims 1-3. Thus, the rejection under 35 U.S.C. § 103(a) should be withdrawn, and Applicants respectfully request that claims 1-3 receive allowance.

Claims 4 and 5 are allowable at least by virtue of their dependency from one of the independent claims, but also because they are distinguishable over the prior art. Applicants respectfully request the withdrawal of the rejection, and the allowance of these claims.

In view of the foregoing, it is submitted that the present application is in condition for allowance and a notice to that effect is respectfully requested. If, however, the Examiner deems that any issue remains after considering this response, the Examiner is invited to contact the undersigned attorney/agent to expedite the prosecution and engage in a joint effort to work out a mutually satisfactory solution.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 19-2380. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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